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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/670,567 | 09/26/2003 | Herbert Taucher | 2002P15288US/ERB | 2326 |

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| EXAMINER | |
|---|---|
| TAT, BINH C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/670,567 | TAUCHER ET AL. | |
| | Examiner | Art Unit | |
| | Binh C. Tat | 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *21 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01/12/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. This office action is in response to application 10/670567 file on 05/21/04.

Claim 1-10 remain pending in the application.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Saueret al. (US Patent 5951704).

3. As to claim 1, Saueret al. teach a method for function testing an emulated logic circuit comprising the step of: loading a model of the logic circuit into a hardware emulator in a hardware description language (see fig 1, fig 2, and fig 7 element 23 col 4 lines 17-64), putting the emulated logic circuit into an operating mode in which some or all of the flip-flop it contains, in particular with additional some logic elements as one or more shift registers (see fig 1, fig2, and fig4 and fig 7 col 4 lines 47 to col5 lines 8, and col 6 lines 1-14 and col 9 lines 16-53), and comparing structural arrangement of the logic circuit in the hardware emulator with structural arrangement of the model of the logic circuit at least partially with the assistance of interfacing circuitry, are functionally chained into the operating mode (see fig 1, fig2, and fig 4 -7 col 4 lines 47 to col 6 lines 14, and col 6 lines 65 to col 7 lines 30 and col 9 lines 16-53).

4. As to claims 2, Saueret al. teach further comprising the step of: applying a test pattern to inputs of the emulator, the emulator inputs representing inputs of shift registers (see fig 1, fig2,

and fig4 and fig 7 col 4 lines 47 to col5 lines 8, and col 6 lines 1-14 and col 9 lines 16-53), and shifting the pattern into the shift registers by means of suitable pulsing (see fig 1, fig2, and fig4 and fig 7 col 4 lines 47 to col5 lines 8, and col 6 lines 1-14 and col 9 lines 16-53), setting the emulated logic circuit to a standard operating mode whereby, one or more pulsing cycles ensue, and the circuit then re-set an original operating mode (see fig 1, fig 2, and fig 7 element 23 col 4 lines 17-64), shifting the ensuing result pattern is means of suitable pulsing to emulator outputs which simultaneously represent outputs of the shift registers, and carrying out a check to determine whether the pattern matches an expected value (see fig 1, fig2, and fig4 and fig 7 col 4 lines 47 to col5 lines 8, and col 6 lines 1-14 and col 9 lines 16-53), and using a check result is compare the structural arrangement of the logic circuit in the hardware emulator with the structural arrangement of the model of the logic circuit (see fig 1, fig2, and fig 4 -7 col 4 lines 47 to col 6 lines 14, and col 6 lines 65 to col 7 lines 30 and col 9 lines 16-53).

5. As to claims 3, Saueret al. teach further comprising the steps of: applying test pattern to an emulator input, the test pattern represents the input of a shift register, and shifting the test pattern through the shift register by means of suitable pulsing (see fig 1, fig2, and fig4 and fig 7 col 4 lines 47 to col5 lines 8, and col 6 lines 1-14 and col 9 lines 16-53), checking an emulator output which simultaneously represents the output of this shift register for the appearance of the test pattern or of an inverted test pattern, determining number of flip-flops in the shih register from a number of pulsing sequences required for shifting through (see fig 1, fig2, and fig4 and fig 7 col 4 lines 47 to col5 lines 8, and col 6 lines 1-14 and col 9 lines 16-53), and using results of the step of determining in a comparison of the structural arrangement of the logic circuit in the hardware emulator with the structural arrangement of the model of the logic circuit (see fig 1,

fig2, and fig 4 -7 col 4 lines 47 to col 6 lines 14, and col 6 lines 65 to col 7 lines 30 and col 9 lines 16-53 and summary and background).

6. As to claims 4, Saueret al. teach further comprising the steps of connecting an output of a shift register to an input of a next adjacent shift register and chaining all shift registers into a single shift register by means of recursion (see fig 1, fig2, and fig4 and fig 7 col 4 lines 47 to col5 lines 8, and col 6 lines 1-14 and col 9 lines 16-53 and background).

7. As to claims 5, Saueret al. teach further comprising the steps of: in the event that the structural arrangement of the logic circuit in the hardware emulator does not match the structural arrangement of the model, carrving out an analysis to determine sources of such faults (see fig 1, fig2, and fig4 and fig 7 col 4 lines 47 to col5 lines 8, and col 6 lines 1-14 and col 9 lines 16-53 and background), and automatically reloading the model of the logic circuit into the hardware emulator with these sources of faults deactivated (see fig 1, fig2, and fig4 and fig 7 col 4 lines 47 to col5 lines 8, and col 6 lines 1-14 and col 9 lines 16-53 and background).

8. As to claims 6, Saueret al. teach a device for testing comprising: an emulated logic circuit, a hardware emulator for emulating a logic circuit present in the form of a model (see fig 1, fig 2, and fig 7 element 23 col 4 lines 17-64), a test pattern generator module arranged to apply a test pattern to an input of the hardware emulator (see fig 3, and fig 4 col 5 lines 9 to col 6 lines 35), a pulse generator arranged to inject a pulse into the hardware emulator (see fig 1, fig 2, and fig 7 col 4 lines 17-64), a test pattern checking module arranged to check whether a bit pattern being applied to an output of the hardware emulator matches an expected value (see fig 1, fig2, and fig4 and fig 7 col 4 lines 47 to col5 lines 8, and col 6 lines 1-14 and col 9 lines 16-53), a module for comparing a structural arrangement of the logic circuit in the hardware emulator with

a structural arrangement of model of the logic circuit at least partially with the assistance of an operating mode of the logic circuit in which some or all of the flip-flops it contains, in particular with additional logic elements as interfacing circuitry, are functionally chained into one or more shift registers (see fig 1, fig2, and fig 4 -7 col 4 lines 47 to col 6 lines 14, and col 6 lines 65 to col 7 lines 30 and col 9 lines 16-53 and summary and background).

9. As to claims 7, Saueret al. teach further comprising a module for determining the number of flip-flops in the shift register from a number of pulse sequences needed to shift a test pattern through the register and a module for briefly changing over the logic circuit to a standard operating mode for one pulse cycle or several pulse cycles while a test pattern is being shifted through the register (see fig 1, fig2, and fig4 and fig 7 col 4 lines 47 to col5 lines 8, and col 6 lines 1-14 and col 9 lines 16-53 and background).

10. As to claims 8, Saueret al. teach further comprising a module for chaining all the shift register into a single shift register by means of recursively connecting the output one shift register to the input a next adjacent shift register (see fig 1, fig2, and fig4 and fig 7 col 4 lines 47 to col5 lines 8, and col 6 lines 1-14 and col 9 lines 16-53 and background).

11. As to claims 9, Saueret al. teach further comprising a module for analyzing the sources of faults leading to a lack of matching between the structural arrangement of the logic circuit in the hardware emulator and the structural arrangement of the model, and a module for automatically loading the model of the logic circuit into the hardware emulator with these sources of faults deactivated (see fig 1, fig2, and fig4 and fig 7 col 4 lines 47 to col5 lines 8, and col 6 lines 1-14 and col 9 lines 16-53 and background).

*12.* As to claims 10, Saueret al. teach further comprising a module for determining the number of flip-flops in the shift register from a number of pulse sequences needed to shift a test pattern through the register or a module for briefly changing over the logic circuit to a standard operating mode for one-pulse cycle or several pulse cycles while a test pattern is being shifted through the register (see fig 1, fig2, and fig4 and fig 7 col 4 lines 47 to col5 lines 8, and col 6 lines 1-14 and col 9 lines 16-53).

***Conclusion***

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Binh C. Tat whose telephone number is (571) 272-1908. The examiner can normally be reached on 7:30 - 4:00 (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Smith can be reached on (571) 272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-1908 for regular communications and (703) 305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Binh Tat
Art unit 2825
July 7, 2005

Paul Dinh